REMARKS

Claims 1, 6-9, 16, and 19-26 are all the claims presently pending in the application. Claims 10-15 stand withdrawn, as resultant from restriction, but are subject to evaluation for rejoinder upon ultimate determination of allowable subject matter.

The Examiner objects to claim 22 as having repetitive numbering. Applicants believe the above claim amendments appropriately address this concern and respectfully request that the Examiner reconsider and withdraw this objection, since the numbering for claims 23-26 has been corrected.

It is noted that the claim amendments, if any, are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1, 6-9, 16, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over US Patent 6,642,539 to Ramesh et al., although it appears that the Examiner intended to include all current claims in this rejection.

This rejection based on Ramesh is again respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described, for example, in independent claim 1, the claimed invention is directed to a storage medium including a metallic underlayer and a ferroelectric data layer over the metallic underlayer that serves as a layer for storing information as polarized domains on the surface of the ferroelectric data layer. A layer over the ferroelectric data layer has a charge migration rate faster than a charge migration rate of the ferroelectric data layer.

As explained at lines 11-17 of page 2 of the specification, no solution has yet been found to the surface depolarization problem that plagues the art of ferroelectric disk technology using vertical polarization of an FE surface, as explained in more detail beginning at line 22 on page 6, wherein is described a slow loss of surface polarization over several to 24 hours time scale. The inventors recognized that this effect was due not to loss of bulk

polarization in the FE film but to accumulation of mobile surface charges which neutralize the bound charges constituting the surface polarization.

The claimed invention provides a solution to this recognition of surface polarization, by providing a layer over the ferroelectric data layer that has a charge migration rate that is faster than the charge migration rate of the ferroelectric data layer and thereby protects against surface depolarization of the polarized domains.

II. THE PRIOR ART REJECTION

The Examiner continues to allege that Ramesh renders obvious the present invention as defined by claims 1, 6-9, 16, 19, and 20. Applicants again respectfully disagree and again respectfully submit that the rejection of record fails to establish a *prima facie* rejection, based on the Examiner's explanation provided in the latest rejection, wherein the Examiner provides an indication of the intended layers of Ramesh considered to be significant in the Examiner's prior art evaluation.

To begin with, Applicants gratefully acknowledge Examiner Harris for finally providing an indication on page 3 of the Office Action mailed on January 29, 2009, as to the basis for the rejection of record, since, as Applicants have repeatedly pointed out, Ramesh is directed to an entirely different memory technology using a transistor/ferroelectric memory capacitor to form the basic memory cell unit.

In contrast, the memory cell unit of the present invention uses polarized domains in the upper surface of a ferroelectric data layer. The present invention will provide far higher storage density than capable with the technology described in Ramesh. That is, as described at line 14 of page 5 of the specification of the present application, the present invention is projected to be capable of 3000 Gb/in^2 (Gigabits per square inch) => 0.215 x 10^{-3} μm^2/bit. In contrast, the ferroelectric RAM, based on a transistor/ferroelectric capacitor, is described on Wikipedia.org as having a typical cell size of 0.22 μm^2, when using the 90 nm process for fabrication. Thus, as a first approximation, and assuming Applicants' representation has calculated correctly, the technology of the claimed invention is roughly three orders of magnitude better in density from that used in Ramesh.

As explained at lines 20-21 of page 6, the problem being addressed by the present invention is that the inventors recognized there to be a slow surface depolarization of the polarization-written information described in their previous patent, US Patent 6,515,957. As

explained at the top of page 7, the inventors were able to discover that this slow loss of surface polarization was not due to a loss of bulk polarization in the FE film, but, rather, was due to accumulation of mobile surface charges which neutralize the bound charge constituting the surface polarization.

The solution offered by the present invention is that of providing an overlying conducting layer (e.g., layer 211 shown in Figure 2), thereby shielding against this depolarization. In an exemplary embodiment, the conducting layer directly contacts the ferroelectric data layer.

Therefore, the type of ferroelectric memory of the present invention is entirely different from the ferroelectric memory cell used in Ramesh, even if there are some co-incidental similarities in some materials of some layers. That is, there is nothing in Ramesh that corresponds to the structure 210 shown in Figure 2 of the present application and as described in the independent claims. Absent such demonstration of corresponding structure, the rejection clearly fails to establish a *prima facie* rejection.

Turning now to the rejection currently of record and the Examiner's figure on page 3 of the Office Action, the Examiner considers that PZT layer 66 corresponds to the FEDL layer 502 and LSCO layer 68 corresponds to CL layer 503. Therefore, as a minimum to address the final limitation of the independent claims, the Examiner's initial burden would be that of demonstrating that LSCO layer 68 has a charge migration rate that is faster than the charge migration rate of PZT layer 66. The Examiner fails to provide this demonstration in the rejection of record.

However, Applicants bring to the Examiner's attention that, regardless of this final claim limitation, the second claim limitation clearly requires that the ferroelectric data layer stores information as polarized domains, which description has been further amended to clarify that the polarized domains are on the surface of this ferroelectric data layer (e.g., reference Figures 1 and 2 of the present Application. As explained at lines 19-20 of page 6, the technology of the present invention has been demonstrated for domains on the scale of 1000Å or less.

As can be seen in Figures 1 and 2, these domain regions are free standing domains on the surface of the FE DL layer that are not dependent upon a transistor/ferroelectric capacitor structure such as shown in Ramesh Figure 8 (as further applied in the structure shown in Figure 9 of Ramesh).

Therefore, given the Examiner's correspondence of layers, the Examiner's initial

burden to establish a *prima facie* rejection for independent claim 1 would be to demonstrate not only that LSCO has a faster charge migration rate than PZT but also to demonstrate that polarized domains are used on the surface of the PZT layer of Ramesh as the data storage layer. However, since the memory cell in Ramesh is based upon the combination of switching transistor/ferroelectric capacitor, its memory cell clearly fails to use polarized domains on the surface of the PZT, as would be required to satisfy the plain meaning of the claim language.

The polarized domains are even further clarified in recently-added dependent claim 21-23.

Along this line, it is noted that the Examiner states on page 2 of the Office Action: "*Applicant argues that the underlayer serves as a layer for storing information as polarized domains in the ferroelectric data layer. However, this would be a process of using said storage medium which in a product claim is given minimal weight.*"

In response, Applicants respectfully submit that the Examiner's above-recited explanation indicates fundamental confusion by the Examiner, as follows.

First, the second claim limitation includes a functional description of the ferroelectric data layer, along with the mechanism used for the data storage (e.g., polarized domains on the surface of the ferroelectric data layer). In contrast, the mechanism used in Ramesh for data storage is clearly shown in Figure 9 as including the combination of the switching transistor S-G-D and the ferroelectric capacitor structure above the transistor, an entirely different mechanism from that described in the independent claims.

Second, functional descriptions of components within a device are completely proper and have complete patentable weight, as clearly demonstrated by MPEP §2114 and MPEP §2173.05(g). The Examiner is perhaps confusing the lack of patentable weight as applied to an intended use of an entire apparatus, as opposed to a functional description of a component within a claimed apparatus.

Third, the Examiner's statement implies that the second claim limitation relates to the process of fabricating this ferroelectric data layer. This implication is also incorrect, since the limitation does not in any way define how this ferroelectric data layer has been fabricated within the claimed storage medium.

Hence, turning to the clear language of the claims, in Ramesh there is no teaching or suggestion of a: "… storage medium, comprising: a metallic underlayer; a ferroelectric data

layer over said metallic underlayer, said ferroelectric data layer serving as a layer for storing information as polarized domains on a surface of said ferroelectric data layer; and a layer over said ferroelectric data layer having a charge migration rate faster than a charge migration rate of said ferroelectric data layer", as required by independent claim 1. The remaining independent claims have similar language.

Therefore, Applicants again respectfully submit that there are features of the claimed invention that are not taught or suggested by Ramesh, and the Examiner is respectfully requested to reconsider and withdraw this rejection based on Ramesh.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1, 6-9, 16, and 19-26, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance, and that withdrawn claims 10-15 are also in condition to be rejoined and allowed, since they are also amended to reflect allowable subject matter. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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